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(21)Application number: 11026643	(71)Applicant:	INTERNATL BUSINESS MACH CORP <IBM>
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(54) METHOD AND SYSTEM FOR MAINTAINING CACHE COHERENCE

(57)Abstract:

PROBLEM TO BE SOLVED: To avoid an unnecessary write operation to a system memory by maintaining cache coherence in a multiprocessor computer system through the use of a coherence state with tag.
SOLUTION: When a changed value is allocated to a cache line which is loaded most recently, a state with tag can be moved by crossing a cache in a horizontal direction. When a request is given for accessing to a block, related priority is given so that only a response having the highest priority is sent to a requesting processing unit. When a cache block is in a change state in one processor and a read operation is requested by the different processor, the first processor sends a change intervention response and a read processor can hold the data in a T state.
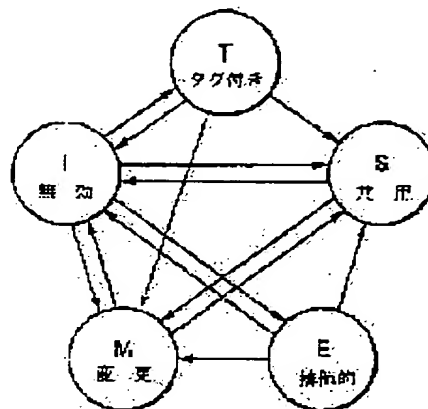
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